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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/071,494
Filing Date	February 6, 2002
First Named Inventor	Taeg-Hyun Kang, et al.
Art Unit	2826
Examiner Name	V. Mandala
Attorney Docket Number	11948.1
Total Number of Pages in This Submission	

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53

- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) ______
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- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please Identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Kirton & McConkie		
Signature	Ken Horton		
Printed name	Kenneth E. Horton		
Date	November 28, 2005	Reg. No.	39,481

CERTIFICATE OF TRANSMISSION/MAILING

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Signature	Erin Cowles		
Typed or printed name	Erin Cowles	Date	November 28, 2005

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Erin Cowles

OIPE DEC 0 1 2005 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/071,494	Confirmation No. 1924
Applicant	:	Taeg-Hyun Kang, et al.	
Filed	:	February 6, 2002	
TC/A.U.	:	2826	
Examiner	:	V. Mandala	
Docket No.	:	11948.1	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

FEE TRANSMITTAL

To Whom It May Concern:

1. **Total Fee Paid: $500.00**

2. **Method of Payment:**

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☐ Deposit Account

Account Number 500843
Account Name Kirton & McConkie

The Director is authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☒ Credit overpayments

☒ Charge any additional fee(s) or any underpayment of fee(s)

to the above-identified deposit account.

3. **Fee For Extra Claims:**

Extra Claims					**Fee/Claim**		**Fee Paid**
Total Claims	31	- 0* =	0	x	50	=	0
Indp. Claims	1	- 0** =	0	x	200	=	0
Multiple Dependent Claims				x	360	=	0

* 20 or highest number of total claims previously paid for.
** 3 or highest number of independent claims previously paid for.

4. Additional Fees:

Fee Description	**Fee Paid**
Surcharge – late filing fee or oath ($130)	
Extension of one month ($120)	
Extension of two months ($450)	
Extension of three months ($1020)	
Extension of four months ($1590)	
Extension of five months ($2160)	
Notice of Appeal ($500)	
Filing appeal brief ($500)	$500
Request for oral hearing ($1000)	
Submission of IDS ($180)	
Record patent assignment ($40)	
RCE ($790)	
Fee for Terminal Disclaimer ($130)	
Fee for extra claims (from above):	
Other: Suspension of Action	
Total:	**$500.00**

Respectfully submitted,

Date: November 28, 2005

By Ken Horton
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Serial No. 10/071,494
Attorney Docket No. 11948-0001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS & INTERFERENCES

In re Patent Application:
Taeg-Hyun Kang, et al.

Serial No.: 10/071,494

Filed: February 6, 2002

For: FIELD TRANSISTORS FOR ELECTROSTATIC DISCHARGE PROTECTION AND METHODS FOR FABRICATING THE SAME

Confirmation No. 1924

Group Art Unit: 2826

Examiner: V. Mandala

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

APPEAL BRIEF

In response to the final Office Action dated March 28, 2005, and further to the Notice of Appeal filed on September 27, 2005, Applicant requests the Board of Appeals and Interferences to reconsider this application and reverse the pending rejections.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on this 28th Day of November 2005.

Signed: ______________________

11/28/2005

1. REAL PARTY IN INTEREST

The real party in interest of record in the present Appeal is Fairchild Korea Semiconductor, Ltd. by virtue of two Assignments from the inventors to Fairchild Semiconductor Corporation and then from that entity to Fairchild Korea Semiconductor, Ltd.

2. RELATED APPEALS & INTERFERENCES

To the best of the undersigned's knowledge, there exists no related appeal or interference.

3. STATUS OF CLAIMS

The pending claims are attached to this Appeal Brief as Appendix A. Briefly, claims 1-41 are pending in this application, with claims 11-18 and 30-39 withdrawn from consideration and claims 1-10, 19-29, and 40-41 finally rejected.

4. STATUS OF AMENDMENTS

No amendments have been proposed or entered after the final Office Action dated March 28, 2005. No amendments are proposed in this Appeal.

5. SUMMARY OF INVENTION

Figure 1 from the present application (attached as Exhibit D) illustrates a conventional semiconductor device used for electrostatic damage (ESD) protection. This device contains a field oxide layer 17 and a patterned gate conductive layer 18 that is formed on a gate insulating layer 19. The gate conductive layer 18 overlaps parts of source region 14 and drain region 15

while overlapping all of field oxide layer 17. A gate electrode 20 is formed on the patterned gate conductive layer 18, and a source electrode 21 contacts both the source region 14 and the diffusion region 16. A drain electrode 22 contacts the drain region 15 and is connected to the gate electrode 20 and an interlayer dielectric layer 23 electrically isolates each electrode. *See [005-006].*

When ESD stress is generated in the drain electrode 22, a turn-on voltage is applied to the gate electrode 20 to form an inversion layer between the source region 14 and drain region 15. The inversion layer provides a complete current path that is able to route the ESD current to the bulk of the device, thereby protecting the devices against the ESD stress. The smaller thickness of a gate insulating layer 19 (relative to the field oxide layer 17) increases the possibility that it will breakdown due to the ESD stress, thereby reducing the reliability of the device. *See [006-009].*

To overcome this problem, the claimed semiconductor device does not contain a thin gate insulating layer. As best shown in Figure 2 of the application (attached as Exhibit E), the gate conductive layer 180 is formed on the relatively-thick field oxide layer 170. Thus, the dielectric destruction of the oxide insulating layer due to the ESD stress does not occur. The ESD protection is still provided by the current path formed by the source region 145 and drain region 155 between source region 140 and the drain region 150. *See [032-033].*

6. ISSUES

A. Whether the Examiner has properly rejected claims 1-10, 19-29, 40 and 41 under 35 U.S.C. § 112, ¶ 2 as being indefinite.

B. Whether the Examiner has properly rejected claims 1-4, 7-10, 19, 23, 26, 27, and 29 under 35 U.S.C. § 102(b) as being anticipated by Murakami et al. (U.S. Patent No. 5,623,154; Exhibit B).

7. GROUPING OF CLAIMS

A. Claims 1-10 stand or fall together.

B. Claims 19-26 stand or fall together.

C. Claims 27-28 stand or fall together.

D. Claim 29 stands alone.

E. Claim 40 stands alone.

F. Claim 41 stands alone.

8. ARGUMENT

A. The 35 U.S.C. § 112 ¶ 2 Rejection

Claims 1-10, 19-29, 40 and 41 stand finally rejected under 35 U.S.C. § 112, ¶ 2 as being indefinite. All of these rejected claims contain the limitation that the claimed semiconductor device (or transistor) has a current path between a source and a drain while containing no thin gate insulating layer. The Examiner has rejected the claims as being indefinite because the present specification does not disclose any numeric limitations about the thickness of the gate oxide layer which would be used as a reference point in defining the difference between thick and thin. *See 3/28/05 Office Action at 3.*

Applicant respectfully disagrees that an exact numerical range needs to be described in the specification for the claim term "thin gate oxide layer" to be definite. To begin with, using a

term of degree (i.e., such as thin) does not automatically render the claim indefinite. *Seattle Box Co., v. Industrial Crating & Packing, Inc.*, 731 F.2d 818, 221 USPQ 568 (Fed. Cir. 1984). When a term of degree is used, the Examiner must first determine whether the specification provides some standard for measuring that degree. But the inquiry does not conclude there. If such a standard is not present, the Examiner must inquire to whether the skilled artisan would still "reasonably" be apprised of the scope of the invention. *See M.P.E.P. § 2173.05(b)*. In the final rejection, however, the Examiner has merely stopped with the first inquiry and argued that "thin" is not definite because the standard for measuring the thickness is not present in the specification, i.e., there exists no numerical range in the specification. But the Examiner has not argued—much less alleged—that the skilled artisan would not have been reasonably apprised of the scope of thin gate oxide layer.

Further, a definiteness inquiry under 35 U.S.C. § 112, ¶ 2 is an objective determination made in the context of whether the scope of the claim is clear to a hypothetical person possessing the ordinary level of skill in the pertinent art. The inquiry is, therefore, whether the claims set out and circumscribe a particular subject matter with a "reasonable" degree of clarity and particularity. And definiteness must be analyzed, not in a vacuum, but in light of: (i) the disclosure of the present application; (ii) the prior art; and (iii) the claim interpretation given by the skilled artisan at the time the invention was made. *See M.P.E.P. § 2173.02*. The Office, however, has primarily focused only on factor (i).

Turning to factor (i), the present specification describes and illustrates in several instances a thin gate oxide layer, describes their functions, and describes the differences between these two elements. *See Paragraphs [007], [008], & [0032-0033]*. While it is true that the specification

does not give an exact thickness (or range of thicknesses) for the gate oxide layer, such information reasonably apprises the skilled artisan of what is a thin and thick gate oxide layer.

Turning to factor (ii), the prior art, Applicant submitted search results showing that at least 42 patents since 1976 have issued with "semiconductor" and "thin gate oxide layer" phrases in the claims. The Examiner considered such evidence to be non-persuasive and contended that merely citing 42 results of a search engines does not reflect what each of the 42 underlying disclosures teach about this claim term. The Examiner cited to Nishida et al. (U.S. Patent No. 3789503) and Hsu et al. (U.S. Patent No. 6841821) as showing a difference of 1600 Angstroms between what each reference describes as a thin gate oxide layer. The Examiner concluded that it would be improper to assume a definite meaning for this term where multiple definitions are taught by the prior art.

Applicant responded by illustrating that the Examiner's reliance on these two patents is not legally or factually sufficient to support the argument of the existence of a wide disparity of thicknesses for a thin gate oxide layer. The time frame for inquiring about indefiniteness is—as noted above—at the time of the invention. In the present application, the "time of the invention" of the present application is currently based on the effective filing date of the application, or early 2001. Nishida et al. (1974), however, is much earlier than this time frame by 27 years and Hsu et al. (2005) is later than this time frame by several years.

More importantly, as any skilled artisan can testify, the size and dimensions of semiconductor devices have been decreasing for many years.[1] Thus, the gate oxide thickness disclosed by Nishida et al. (in 1974) would necessarily be different (i.e., larger) than the gate

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[1] Indeed, this knowledge is recognized even outside the semiconductor art.

oxide thickness disclosed by Hsu et al. (in 2005). Indeed, the skilled artisan would have expected such a wide difference because of the trends in semiconductor technology. Thus, the disclosures of 2 patents more than 30 years apart does not adequately show the teachings of the prior art (which must be considered when analyzing definiteness).

Perhaps the most pertinent evidence submitted by Applicant is U.S. Patent No. 6,586,306 ("the '306 Patent"; attached as Exhibit F). The '306 Patent has an effective filing date at nearly the same time as the present application. The '306 Patent which contains a claim for making a semiconductor device, including the steps of forming a "thin gate oxide layer" in one region and a "thick gate oxide layer" in another region. Importantly, despite the existence of these two claim terms, there exists no numerical range for "thin" or "thick" in the specification of the '306 Patent, at least none that the undersigned could locate. Yet the '306 Patent was allowed with both of these terms in the claims.

Thus, the Office itself has previously issued claims with the exact same term as recited in the present claims, yet where there also existed no numerical range in the specification. How can an application with "thin gate oxide layer" and no numerical range in the specification be issued as the '306 Patent (and therefore, by definition, be valid and definite) on the one hand, yet on the other hand be deemed not definite? It seems both an illogical and an untenable position.

Further, a cursory review of the previously cited 42 patents showed that the '306 Patent was not an aberration. The Office also issued U.S. Patent No. 6,124,172 (attached as Exhibit G) that contained the term "thin gate oxide layer" in the claims, but without a numerical range for the thickness present in the specification. It is no doubt likely that Applicant could presumably find additional examples in the prior art, e.g., by additional analysis and/or by changing the search parameters. But two patents are sufficient to illustrate that the claims set out and

circumscribe a particular subject matter with a reasonable degree of clarity and particularity in light of the prior art.

Turning to factor (iii) of M.P.E.P. § 2173.02, would the skilled artisan have understood that "thin" gate oxide layer sets out and circumscribes a particular subject matter with a "reasonable" degree of clarity and particularity? To that end, Applicant filed a 37 C.F.R. § 1.132 Declaration evidencing that the skilled artisan would have understood that a "thin gate oxide layer" is reasonably clear and precise. *See Exhibit C.*

Considering all of the evidence, it is clear that the Examiner has not met the requisite burden of showing that "thin gate oxide layer" would render the claims indefinite to the skilled artisan. Accordingly, Applicant respectfully requests the Board to overrule the Examiner and withdraw this rejection.

B. The Rejection over Murakami et al.

Claims 1-4, 7-10, 19, 23, 26, 27, and 29 under 35 U.S.C. § 102(b) stand rejected as being anticipated by Murakami et al. (U.S. Patent No. 5,623,154). The Office argues that Murakami et al. teach the claimed invention in the device depicted in Figure 1 of this prior art reference.

As evident from Exhibit A, the independent claims contain the limitation that the transistor has a current path between a source and a drain while containing no thin gate insulating layer. As described in paragraphs [011] and [032-033] of the present specification, the transistor described contains an inversion layer (135) that provides a current path between the source and drain regions, yet without using a thin gate insulating layer, thereby protecting against ESD stress. The prior art devices (as illustrated in Figure 1) were unable to protect against the ESD

stress because the thin gate insulating layer (19) in the transistor would break down. *See also paragraphs [007] and [008].*

The Examiner has not substantiated that Murakami et al. discloses this limitation in the rejected independent claims. This reference discloses an NMOS transistor 20 containing source and drain regions 11, a gate oxide film 15, and a gate electrode layer 17. *See column 1, lines 25-50 and Figure 1.* As recognized by the skilled artisan and as supported in the remainder of Murakami et al., the gate oxide film 15 would operate as a thin gate insulating layer of the NMOS transistor. Indeed, based on the structure of the NMOS transistor 20 depicted in Figure 1 of Murakami et al., it would be difficult—if not impossible—for the Examiner to substantiate that NMOS transistor 20 contains no thin gate insulating layer.

The Examiner argues that Murakami et al. describe a field transistor with the claimed features and containing "no gate insulating layer." But this is not what the claims recite. The rejected claims recite "no <u>thin</u> gate insulating layer." It appears that the Examiner has ignored the presence of the term "thin," presumably because of the indefiniteness rejection.

But the Examiner can not eliminate this term from the claim when rejecting the claims over Murakami et al. All words in a claim must be considered in judging the patentability of a claim against the prior art. *In re Wilson*, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970). Where the degree of uncertainty about the definiteness of a claim term is not great, the Examiner should reject the claims based on indefiniteness and based on prior art, but "based on the interpretation of the claims which renders the prior art applicable." *See M.P.E.P. § 2173.06; cf Ex parte Ionescu*, 222 USPQ 537 (Bd. App. 1984). When making a rejection over prior art in these circumstances, it is important for the Examiner to point out how the claim is being interpreted.

See M.P.E.P. § 2173.06. But nowhere is the Examiner allowed to just ignore the claim term altogether.

The Examiner, however, has failed to adhere to these standards. Accordingly, the Examiner has not substantiated that Murakami et al. teach each and every limitation in the rejected claims. Accordingly, Applicant respectfully requests the Board to reverse the Examiner and withdraw this ground of rejection.

Applicant notes—for the record—that it requested repetition of the final rejection in accordance with M.P.E.P. § 2173.06. *See 7/28/05 Request for Reconsideration at 7.* The Examiner did not honor this request.

C. Additional Claims Allowable

The above discussion describes the limitations present in all of the pending independent claims, but focuses on those limitations present in claim 40. The remaining independent claims, however, contain limitations that make them separately patentable from claim 40.

Claims 1-10 are separately patentable because they contain the additional components recited therein. The Examiner has not substantiated that Murakami et al. teach or suggest such components.

Claims 19-26 are separately patentable because they contain the additional components recited therein. The Examiner has not substantiated that Murakami et al. teach or suggest such components.

Claims 27-28 are separately patentable because they contain the additional components recited therein. The Examiner has not substantiated that Murakami et al. teach or suggest such components.

Claim 29 is separately patentable because it recites a system for ESD protection, as well the additional components recited therein. The Examiner has not substantiated that Murakami et al. teach or suggest such components.

Claim 41 is separately patentable because it recites a system for ESD protection. The Examiner has not substantiated that Murakami et al. teach or suggest such a feature.

9. CONCLUSION

For the reasons set forth above, as well as those previously of record, Applicant respectfully requests the Board to reverse the Examiner's rejections of the pending claims.

If there is any fee due in connection with the filing of this Appeal, including a fee for any extension of time not accounted for above, please charge the fee to our Deposit Account No. 50-0843.

Respectfully Submitted,

By __________________________

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Date: November 28, 2005

APPENDICES

A. Pending Claims

B. Murakami et al. (U.S. Patent No. 5,623,154)

C. 37 C.F.R. § 1.132 Declaration

D. Figure 1 (prior art device; copied from present application)

E. Figure 2 (inventive device; copied from present application)

F. U.S. Patent No. 6,586,306

G. U.S. Patent No. 6,124,172

Appendix A: Pending Claims

1. A field transistor having a current path between a source and a drain while containing no thin gate insulating layer, the transistor comprising:

a well region of a first conductivity type;

a field oxide layer for defining an active region on the well region;

high concentration source and drain regions of a second conductivity type separated from each other by a width of the field oxide layer;

a low concentration source region of the second conductivity type formed in the well region, the low concentration source region being adjacent to the high concentration source region and overlapped by one end of the field oxide layer;

a low concentration drain region of the second conductivity type formed in the well region, the low concentration drain region being adjacent to the high concentration drain region and overlapped by the other end of the field oxide layer; and

a gate conductive layer pattern formed on the field oxide layer, the gate conductive layer pattern overlapping parts of the low concentration source and drain regions of the second conductivity type.

2. The field transistor of claim 1, wherein the well region of the first conductivity type is formed on a high concentration buried region of the first conductivity type on a semiconductor substrate of the first conductivity type.

3. The field transistor of claim 1, wherein the well region of the first conductivity type is formed on a semiconductor substrate of the first conductivity type.

4. The field transistor of claim 1, further comprising a high concentration diffusion region of the first conductivity type formed in the well region, the high concentration diffusion region being separated from the high concentration source region of the second conductive type by a predetermined distance.

5. The field transistor of claim 4, further comprising a low concentration diffusion region of the first conductivity type and a low concentration diffusion region of the second conductivity type, both low concentration diffusion regions being adjacent to each other between the high concentration diffusion region of the first conductivity type and the high concentration source region of the second conductivity type.

6. The field transistor of claim 5, wherein the low concentration diffusion region of the first conductivity type is adjacent to the high concentration diffusion region of the first conductivity type, and the low concentration diffusion region of the second conductivity type is adjacent to the high concentration source region of the second conductivity type.

7. The field transistor of claim 1, further comprising:

a gate electrode electrically connected to the gate conductive layer pattern;

a source electrode electrically connected to the high concentration source region of the second conductivity type; and

a drain electrode electrically connected to the high concentration drain region of the second conductivity type.

8. The field transistor of claim 7, wherein the drain electrode is electrically connected to the gate electrode.

9. The field transistor of claim 7, wherein the source electrode is electrically connected to the high concentration diffusion region of the first conductivity type as well.

10. The field transistor of claim 1, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

11. (withdrawn)

12. (withdrawn)

13. (withdrawn)

14. (withdrawn)

15. (withdrawn)

16. (withdrawn)

17. (withdrawn)

18. (withdrawn)

19. A semiconductor device having a current path between a source and a drain while containing no thin gate insulating layer, the transistor comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over a portion of the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer; and

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region.

20. The device of claim 19, further comprising a first diffusion region of the first conductivity type formed in the well region and separated from the first source region.

21. The device of claim 20, further comprising a second diffusion region having a first conductivity type concentration lower than the first diffusion region and comprising a third diffusion region of the second conductivity type, both the second and third diffusion regions adjacent each other and located between the first diffusion region and the first source region.

22. The device of claim 21, the second diffusion region type located adjacent the first diffusion region and the third diffusion region located adjacent the first source region.

23. The device of claim 19, further comprising:

a gate electrode electrically connected to the conductive layer;

a source electrode electrically connected to the first source region; and

a drain electrode electrically connected to the first drain region.

24. The device of claim 23, the drain electrode being electrically connected to the gate electrode.

25. The device of claim 23, the source electrode being electrically connected to the first diffusion region.

26. The device of claim 19, wherein the first conductivity type is p-type and the second conductivity type is n-type.

27. A semiconductor device having a current path between a source and a drain while containing no thin gate insulating layer, the transistor comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer;

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region;

a gate electrode electrically connected to the conductive layer;

a source electrode electrically connected to the first source region; and

a drain electrode electrically connected to the first drain region.

28. The device of claim 27, further comprising a first diffusion region of the first conductivity type formed in the well region and separated from the first source region, a second diffusion region having a first conductivity type concentration lower than the first diffusion region, and a third diffusion region of the second conductivity type, wherein both the second and third diffusion regions are adjacent each other and located between the first diffusion region and the first source region.

29. A system for electrostatic discharge protection containing a field transistor having a current path between a source and a drain without a thin gate insulating layer, the field transistor comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer; and

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region.

30. (withdrawn)

31. (withdrawn)

32. (withdrawn)

33. (withdrawn)

34. (withdrawn)

35. (withdrawn)

36. (withdrawn)

37. (withdrawn)

38. (withdrawn)

39. (withdrawn)

40. A semiconductor device for electrostatic discharge protection, the device comprising a field transistor having both a source region and a drain region overlapped by a gate conductive layer and having a current path between the source region and the drain region while containing no thin gate insulating layer.

41. A system for electrostatic discharge protection, the system comprising a field transistor having both a source region and a drain region overlapped by a gate conductive layer and having a current path between the source region and the drain region while containing no thin gate insulating layer.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application:
Taeg-Hyun Kang, et al.

Serial No.: 10/071,494

Filed: February 6, 2002

For: FIELD TRANSISTORS FOR ELECTROSTATIC DISCHARGE PROTECTION AND METHODS FOR FABRICATING THE SAME

Confirmation No. 1924

Group Art Unit: 2826

Examiner: V. Mandala

Mail Stop After-Final Response
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

DECLARATION UNDER 37 C.F.R. § 1.132

I, the undersigned, declare that:

1. I am one of the inventors of the subject matter in the above-captioned patent application;

2. I have been informed that the claims have not been allowed because the Examiner considers the phrase "thin gate insulating layer" to not be definite because there exists no numerical range of the thickness of the layer in the specification.

3. I consider myself to be "one with ordinary skill in the art" in the semiconductor industry. I base this consideration on my qualifications, which include a B.S. in Applied

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on this 28th Day of June, 2005.

Signed: Erin Cowles

Engineering from the Samsung Institute of Management and Technology. I majored in electrical engineering at the University of Incheon as a part time student and acquired a wide knowledge of integrated circuit design, methodology, and fabrication, as well as programming languages, ESD cell device optimization, and RF simulation. I have also acquired a wide knowledge in the integrated chip design industry through more than 14 years of maintaining and supporting TCAD software.

4. In a transistor of a semiconductor device, the gate insulating layer (usually silicon dioxide and therefore a gate oxide layer) lies between the gate electrode, which turns the current flow on and off, and the channel through which this current flows. The gate oxide layer, in essence, acts as an insulator, protecting the channel from the gate electrode and preventing a short circuit.

5. By reducing the thickness of the gate oxide layer, it is possible to increase the transistor's switching speed. That result is due to the electrode being even closer to the channel, thereby inducing a larger current to flow through the transistor. However, thinner oxide layers degrade at lower voltages, and their behavior is more difficult to understand than the behavior of thicker oxides. As a result, the dimensions of a gate oxide layer are thin enough to assure the performance of the transistor and not under such a high electric field to induce its degradatation, whether a field oxide is thick enough to isolate transistors.

6. A thin gate oxide is formed on an active region that is defined by the field oxide in the substrate. Accordingly, a field transistor with no thin gate oxide can be understood as a field transistor of which the gate electrode does not extend onto the active region. Therefore, the thin gate oxide (considered to be formed on the active region) is distinguished from the field oxide.

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7. That all statements are made of my own knowledge are true and all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

TaegHyun KANG 06/27/05

Name Date

FIG. 1 (PRIOR ART)

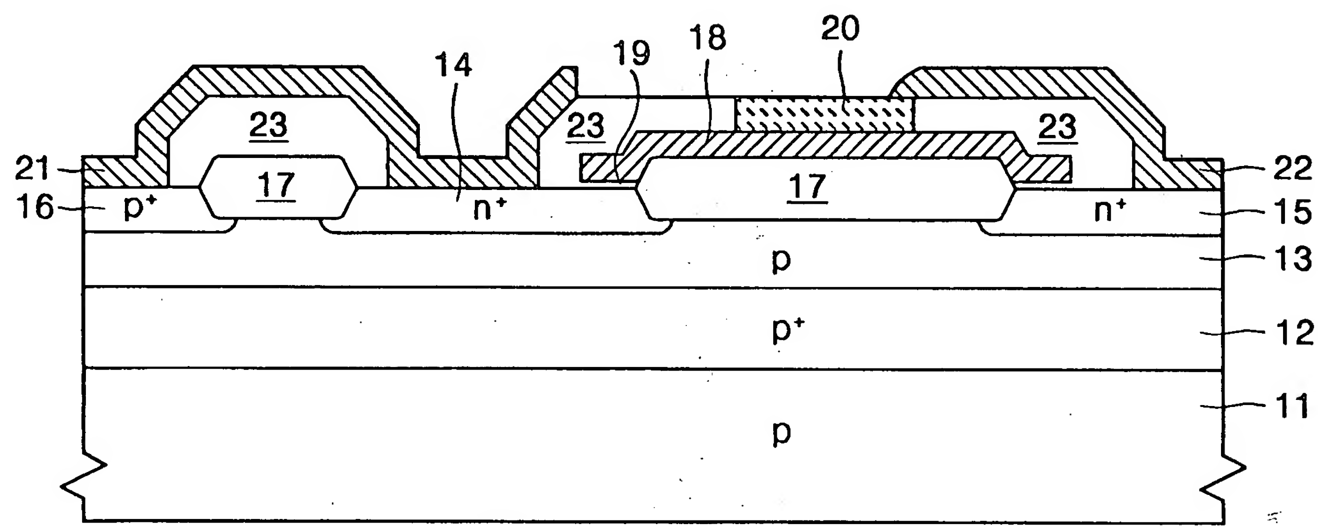
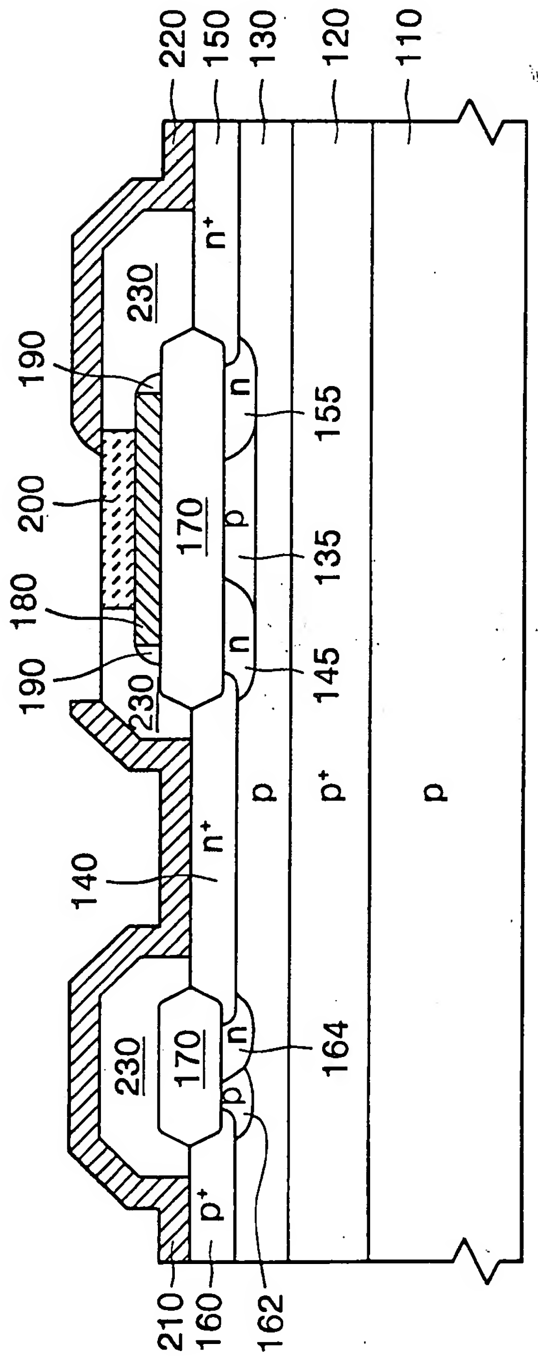


FIG. 2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